IN THE CLAIMS:

Please amend the claims as follows:

Claim 1-6 (Canceled).

Claim 7 (Currently Amended): A photo-detecting apparatus ~~according to claim 1~~ comprising:

a photo-detecting section having: a plurality of pixels arranged in a two-dimensional array having M rows and N columns (M and N each represent an integer of 2 or more) and each having a first photodiode $PD_{A,m,n}$ and a second photodiode $PD_{B,m,n}$; a plurality of lines $L_{A,m}$ provided for the respective rows so that the N first photodiodes $PD_{A,m,1}$ to $PD_{A,m,N}$ included in the group of pixels constituting the m-th row ("m" represents any integer of 1 to M) of the two-dimensional array are electrically connected to each other through the line $L_{A,m}$; and a plurality of lines $L_{B,n}$ provided for the respective columns so that the M second photodiodes $PD_{B,1,n}$ to $PD_{B,M,n}$ included in the group of pixels constituting the n-th column ("n" represents any integer of 1 to N) of the two-dimensional array are electrically connected to each other through the line $L_{B,n}$; and

a signal processing section including M readout circuits $R_{A,1}$ to $R_{A,M}$ and N readout circuits $R_{B,1}$ to $R_{B,N}$, said signal processing section transferring an electric charge generated in said first photodiode $PD_{A,m,n}$ connected to said line $L_{A,m}$ into said readout circuit $R_{A,m}$ to output a voltage value in accordance with the charge quantity in said readout circuit $R_{A,m}$, while transferring an electric charge generated in said second photodiode $PD_{B,m,n}$ connected to said line

$L_{B,n}$ into said readout circuit $R_{B,n}$ to output a voltage value in accordance with the charge quantity in said readout circuit $R_{B,n}$,

wherein said signal processing section further includes M holding circuits $H_{A,1,1}$ to $H_{A,M,1}$, M holding circuits $H_{A,1,2}$ to $H_{A,M,2}$, M holding circuits $H_{A,1,3}$ to $H_{A,M,3}$, M holding circuits $H_{A,1,4}$ to $H_{A,M,4}$, N holding circuits $H_{B,1,1}$ to $H_{B,N,1}$, N holding circuits $H_{B,1,2}$ to $H_{B,N,2}$, N holding circuits $H_{B,1,3}$ to $H_{B,N,3}$, N holding circuits $H_{B,1,4}$ to $H_{B,N,4}$, a first ~~adding and~~ subtracting circuit, and a second ~~adding and~~ subtracting circuit,

wherein one of said holding circuit $H_{A,m,1}$, said holding circuit $H_{A,m,2}$, said holding circuit $H_{A,m,3}$, and said holding circuit $H_{A,m,4}$ holds a voltage value to be outputted from said readout circuit $R_{A,m}$,

wherein one of said holding circuit $H_{B,n,1}$, said holding circuit $H_{B,n,2}$, said holding circuit $H_{B,n,3}$, and said holding circuit $H_{B,n,4}$ holds a voltage value to be outputted from said readout circuit $R_{B,n}$,

wherein said first ~~adding and~~ subtracting circuit receives a voltage value $V_{A,m,1}$ to be outputted from said holding circuit $H_{A,m,1}$, a voltage value $V_{A,m,2}$ to be outputted from said holding circuit $H_{A,m,2}$, a voltage value $V_{A,m,3}$ to be outputted from said holding circuit $H_{A,m,3}$, and a voltage value $V_{A,m,4}$ to be outputted from said holding circuit $H_{A,m,4}$ to output a voltage value representing the ~~addition and~~ subtraction of the voltage values $((V_{A,m,3} - V_{A,m,4}) - (V_{A,m,1} - V_{A,m,2}))$, and

wherein said second ~~adding and~~ subtracting circuit receives a voltage value $V_{B,n,1}$ to be outputted from said holding circuit $H_{B,n,1}$, a voltage value $V_{B,n,2}$ to be outputted from said holding circuit $H_{B,n,2}$, a voltage value $V_{B,n,3}$ to be outputted from said holding circuit $H_{B,n,3}$, and a voltage

value $V_{B,n,4}$ to be outputted from said holding circuit $H_{B,n,4}$ to output a voltage value representing ~~said addition and~~ the subtraction of the voltage values $((V_{B,n,3} - V_{B,n,4}) - (V_{B,n,1} - V_{B,n,2}))$.

Claim 8 (Currently Amended): A photo-detecting apparatus ~~according to claim 1~~ comprising:

a photo-detecting section having: a plurality of pixels arranged in a two-dimensional array having M rows and N columns (M and N each represent an integer of 2 or more) and each having a first photodiode $PD_{A,m,n}$ and a second photodiode $PD_{B,m,n}$; a plurality of lines $L_{A,m}$ provided for the respective rows so that the N first photodiodes $PD_{A,m,1}$ to $PD_{A,m,N}$ included in the group of pixels constituting the m-th row ("m" represents any integer of 1 to M) of the two-dimensional array are electrically connected to each other through the line $L_{A,m}$; and a plurality of lines $L_{B,n}$ provided for the respective columns so that the M second photodiodes $PD_{B,1,n}$ to $PD_{B,M,n}$ included in the group of pixels constituting the n-th column ("n" represents any integer of 1 to N) of the two-dimensional array are electrically connected to each other through the line $L_{B,n}$; and

a signal processing section including M readout circuits $R_{A,1}$ to $R_{A,M}$ and N readout circuits $R_{B,1}$ to $R_{B,N}$, said signal processing section transferring an electric charge generated in said first photodiode $PD_{A,m,n}$ connected to said line $L_{A,m}$ into said readout circuit $R_{A,m}$ to output a voltage value in accordance with the charge quantity in said readout circuit $R_{A,m,}$ while transferring an electric charge generated in said second photodiode $PD_{B,m,n}$ connected to said line $L_{B,n}$ into said readout circuit $R_{B,n}$ to output a voltage value in accordance with the charge quantity in said readout circuit $R_{B,n}$,

wherein said signal processing section further includes M holding circuits $H_{A,1,1}$ to $H_{A,M,1}$, M holding circuits $H_{A,1,2}$ to $H_{A,M,2}$, M holding circuits $H_{A,1,3}$ to $H_{A,M,3}$, M holding circuits $H_{A,1,4}$ to $H_{A,M,4}$, N holding circuits $H_{B,1,1}$ to $H_{B,N,1}$, N holding circuits $H_{B,1,2}$ to $H_{B,N,2}$, N holding circuits $H_{B,1,3}$ to $H_{B,N,3}$, N holding circuits $H_{B,1,4}$ to $H_{B,N,4}$, and ~~an adding and~~ a subtracting circuit,

wherein one of said holding circuit $H_{A,m,1}$, said holding circuit $H_{A,m,2}$, said holding circuit $H_{A,m,3}$, and said holding circuit $H_{A,m,4}$ holds a voltage value to be outputted from said readout circuit $R_{A,m}$,

wherein one of said holding circuit $H_{B,n,1}$, said holding circuit $H_{B,n,2}$, said holding circuit $H_{B,n,3}$, and said holding circuit $H_{B,n,4}$ holds a voltage value to be outputted from said readout circuit $R_{B,n}$, and

wherein said ~~adding and~~ subtracting circuit receives a voltage value $V_{A,m,1}$ to be outputted from said holding circuit $H_{A,m,1}$, a voltage value $V_{A,m,2}$ to be outputted from said holding circuit $H_{A,m,2}$, a voltage value $V_{A,m,3}$ to be outputted from said holding circuit $H_{A,m,3}$, and a voltage value $V_{A,m,4}$ to be outputted from said holding circuit $H_{A,m,4}$ to output a voltage value representing ~~said addition and~~ the subtraction of the voltage values $((V_{A,m,3} - V_{A,m,4}) - (V_{A,m,1} - V_{A,m,2}))$ as well as receiving a voltage value $V_{B,n,1}$ to be outputted from said holding circuit $H_{B,n,1}$, a voltage value $V_{B,n,2}$ to be outputted from said holding circuit $H_{B,n,2}$, a voltage value $V_{B,n,3}$ to be outputted from said holding circuit $H_{B,n,3}$, and a voltage value $V_{B,n,4}$ to be outputted from said holding circuit $H_{B,n,4}$ to output a voltage value representing ~~said addition and~~ the subtraction of the voltage values $((V_{B,n,3} - V_{B,n,4}) - (V_{B,n,1} - V_{B,n,2}))$.